

Constantine Vasilakis

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EDUCATION

University of Illinois Urbana-Champaign

Champaign, Illinois

Bachelor of Science in Computer Engineering

Expected May 2028

Minor in Semiconductor Engineering and Music

IEEE-HKN Honor Society, Samsung Technology Track Scholarship Recipient

- **Relevant Coursework:** Computer Organization & Design (Comp Arch), VLSI System Design (PD), Computer Systems Engineering (OS), Digital Systems Laboratory (FPGA/RTL), Data Structures, Semiconductor Electronics

SKILLS

- **Languages:** SystemVerilog, Verilog, VHDL, C, C++, Python, TCL, Assembly (RISC-V, LC-3)
- **Design:** RTL/microarchitecture, ASIC/FPGA design, testbenches, synthesis, STA, CDC, P&R, DRC/LVS
- **Tools:** Synopsys Design Compiler/VCS/Verdi, Cadence Virtuoso/Innovus, Vivado/Vitis, Verilator, gem5, Spike

PROJECTS

Superscalar Out-of-Order RV32IM Processor

3-Person Team, 2026

SystemVerilog, RISC-V, RTL/Microarchitecture, Synopsys Design Compiler/VCS/Verdi, Verilator, Spike

- Placed **3rd of 33 teams** in ECE 411 OoO competition with $\sim 2\times$ baseline IPC and geometric-mean **PD⁴ of 46.85**
- Co-designed a **2-wide superscalar OoO core** with PRF, ROB, RAT, issue queue, split LSQ, and **4 CDBs**
- Closed synthesis timing at **599.16 MHz** in FreePDK45 with **283,660 μm^2** cell area using Design Compiler
- Architected a **split LSQ** with load disambiguation, raising AES-SHA to **0.8 IPC**, a class record
- Built a **GShare** predictor with speculative GHR and RAS, improving accuracy **55.5pp** over static not-taken
- Verified RV32IM architectural state using an **RVFI monitor** cross-checked against the **Spike ISA reference**

Bit-Sliced RV32I Processor with Full-Custom Layout and Place & Route

2026

Cadence Virtuoso/Innovus, Synopsys VCS, FreePDK45, VLSI Physical Design, STA, DRC/LVS, TCL

- Designed a 32-bit **bit-sliced RISC-V datapath** spanning custom schematics, transistor layout, and digital control
- Hand-laid **35,584 transistors** in a $79.1\times 102.4\mu\text{m}$ core with **8,097 μm^2** area, DRC/LVS clean
- Routed control, carry, and data across **6 metal layers** in FreePDK45 using manual floorplanning and custom layout
- Placed and routed the control unit in **Cadence Innovus** and performed post-layout **static timing analysis**

NES Hardware Emulator SoC on FPGA

2-Person Team, 2025

SystemVerilog, Xilinx Vivado, Spartan-7 FPGA, SoC Design, Clock Domain Crossing

- Designed an NES **SoC** integrating 6502 CPU, custom PPU/APU, DMA, memory-mapped I/O, and bus interconnect
- Built a scanline PPU with tile shifters, **6-state sprite evaluation FSM**, and priority-based pixel compositing
- Drove **21/25/125 MHz** domains with MMCMs, **2-flop synchronizers**, and async FIFOs for safe CDC
- Implemented **OAM DMA**, memory-mapped I/O, and CPU/PPU/APU bus arbitration across the FPGA SoC

RESEARCH

Criticality-Based Load Value Prediction

Sep 2026 – Present

Undergraduate Researcher, advised by Dr. David Schall, Imperial College London

gem5, C++, Python, Arm ISA, Computer Architecture, Performance Modeling

- Extending **gem5 O3CPU** load value prediction for Arm by analyzing and building on a stride-based predictor
- Implementing the **EVES value predictor** (CVP-1 winner) as a gem5 SimObject using **TAGE** components
- Evaluating prediction accuracy and **IPC impact** with targeted microbenchmarks under atomic and O3 CPU models

WORK EXPERIENCE

Course Assistant, Digital Systems Laboratory

Champaign, Illinois

University of Illinois Urbana-Champaign

January 2026 – Present

- Mentoring **300+** students in **SystemVerilog RTL, FPGA design, and digital logic** during office hours
- Teaching the **Vivado simulation/synthesis flow** while debugging SystemVerilog and embedded C with students
- Guiding students through **simulation, synthesis, timing analysis, and on-board FPGA debugging**

Course Staff, Computer Systems & Programming

Champaign, Illinois

University of Illinois Urbana-Champaign

August 2025 – Present

- Evaluating ~ 30 weekly LC-3/C/C++ assignments and providing technical feedback on correctness and code quality
- Tested and migrated Honors MPs from **LC-3 to RISC-V**, validating functionality across the new ISA
- Helping lead comprehensive review sessions covering low-level programming and computer systems concepts